

x86 IA Processor

PRODUCT BRIEF

***iDragon*TM mP6 IA Processor Overview**

The RiseTM *iDragon*TM mP6 IA processor is the first sixth generation x86-compatible processor optimized for low power consumption, high-performance information appliance applications such as set-top box, internet box, thin client, home gateway, IPVR and others. The innovative *iDragon*TM mP6 IA processor is a superscalar and superpipelined IA processor featuring 3 integer units, 3-way MMX technology and a fully pipelined floating point unit giving the users the utmost JAVA*, multimedia, video streaming and browsing experiences. The innovative circuitry of the *iDragon*TM mP6 IA processor is optimized for low power consumption with the highest execution parallelism, which provides the excellent system thermal efficiency for enhanced system reliability.



- **x86 Instruction Set Enhanced with MMXTM Technology**
- **Superscalar and Superpipelined Integer and MMX Architecture**
 - Excellent JAVA*, Multimedia, and Browsing Performance
 - Efficient MPEG4 Video Streaming
- **Advanced On-chip and System Power Management for Excellent Thermal Efficiency and Reliability**
 - Facility Gating
 - Required Selection Only
 - Necessity Switching Only
 - SMM Compatible
 - Clock Control
 - ACPI Compliant
- **Advanced Architectural Features**
 - Advanced Data Dependency Removal Techniques
 - Innovative Instruction Decode and Branch Prediction
 - Dynamic Allocation of Resources
- **Separate Code and Data Caches**
 - 8KB Code and 8KB Data
 - Filtered Tag Prefetching
 - Split Line Access Mechanism
- **High Performance FPU**
 - IEEE 854 Compliant
 - 80 Bit or 64 Bit Precision Results
- **IEEE 1149.1 Boundary Scan**
- **ISO 9001 Wafer Fabrication, Assembly and Test**
- **Support for Bus Frequencies of 60, 66, 75, 83, 95, and 100 MHz**
- **CPU/Host Bus Ratio 2X, 2.5X, 3X, 3.5X**
- **Low Profile 387-Terminal BGA Package**
- **0.18um CMOS Technology with 3.3V I/O and 2.0V Core**

The diagram illustrates the internal components and data flow of a processor. At the top, the **Branch Target Buffer** and **I Cache** (containing a **TLB**) are connected to the **A/D** (Address/Data) bus. The **I Cache** feeds into the **Instruction Buffer**. The **Instruction Buffer** distributes instructions to the **Microcode Unit** and three **Decoder** units. A central horizontal bus connects these units to the **Control**, **Branch Unit**, **Address Generators** (multiple units), and **Registers**. The **Registers** are further divided into **FPU**, **FXCH**, and **MMX** units. The **Control** unit manages the **Integer Registers**. The **Branch Unit** and **Address Generators** interact with the **Integer ALU's**. The **Address Generators** also feed into the **D Cache** (which includes a **TLB**). The **Integer ALU's** and **D Cache** are connected to the **Integer Registers**. The **D Cache** is also connected to the **Registers** and the **A/D** bus.

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